AS1374

200mA, Ultra-Low-Noise, High-PSRR, Dual Low Dropout Regulators

1 General Description

The AS1374 is a ultra-low-noise, low-dropout linear regulator with two seperated outputs. Specifically designed to deliver 200mA continuous output current at each output pin. The LDOs can achieve a low 120mV dropout for 200mA load current and are designed and optimized to work with low-cost, small-capacitance ceramic capacitors.

An integrated P-channel MOSFET pass transistor allows the devices to maintain extremely low quiescent current (30µA).

The AS1374 uses an advanced architecture to achieve ultra-low output voltage noise of 20µVRMS and a power-supply rejection-ratio of better than 85dB (@ 1kHz).

Two active-High enable pins allows to switch on or off each output independently from each other.

The AS1374 requires only 1µF output capacitor for stability at any load.

The device is available in a 6-bump WLP package.

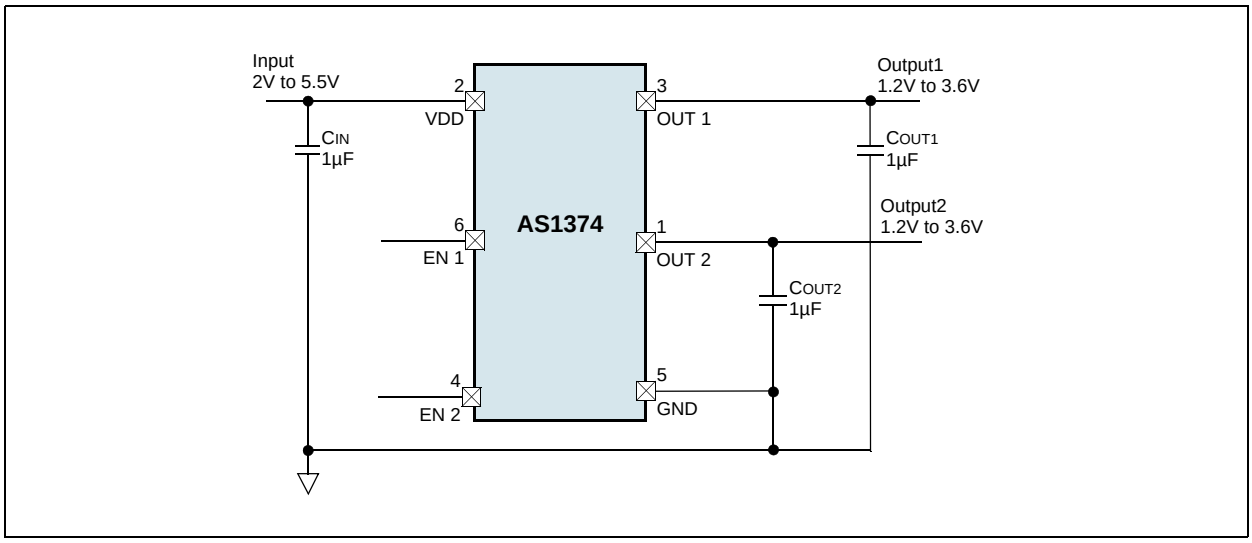
2 Key Features

- Preset Output Voltages: 1.2 to 3.6V (in 50mV steps)
- Output Noise: 20µVRMS @ 100Hz to 100kHz
- Power-Supply Rejection Ratio: 85dB @ 1kHz
- Low Dropout: 120mV @ 200mA Load
- Stable with 1µF Ceramic Capacitor for any Load
- Guaranteed 200mA Output
- Pull-Down Option in Shutdown (factory set)
- Extremely-Low Quiescent Current: 30µA
- Excellent Load/Line Transient
- Overcurrent and Thermal Protection
- 6-bump WLP Package

3 Applications

The devices are ideal for mobile phones, wireless phones, PDAs, handheld computers, mobile phone base stations, Bluetooth portable radios and accessories, wireless LANs, digital cameras, personal audio devices, and any other portable, battery-powered application.

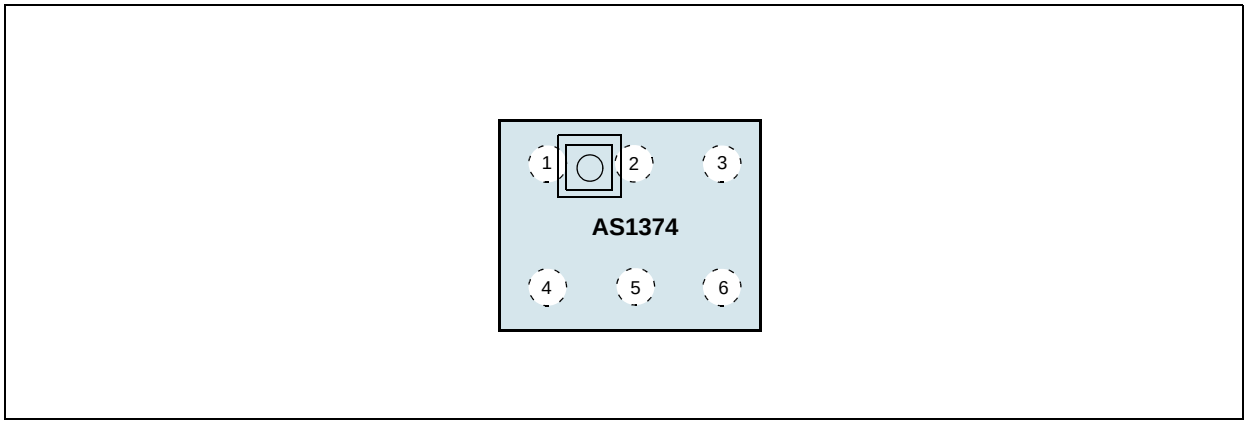
Figure 1. AS1374 - Typical Application Circuit



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	OUT 2	**Regulated Output Voltage 2.** Bypass this pin with a capacitor to GND. See **Capacitor Selection and Regulator Stability on page 11** for more details.
2	VDD	**Input Supply**
3	OUT 1	**Regulated Output Voltage 1.** Bypass this pin with a capacitor to GND. See Capacitor Selection and Regulator Stability on page 11 for more details.
4	EN 2	**Enable 2.** Pull this pin to logic low to disable Regulated Output 2 voltage.
5	GND	**Ground**
6	EN 1	**Enable 1.** Pull this pin to logic low to disable Regulated Output 1 voltage.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD to GND	-0.3	+7	V	
OUT 1, OUT 2, EN 1, EN 2 to GND	-0.3	VDD + 0.3	V	
Output Short-Circuit Duration		Infinite		
ESD	2		kV	*HBM MIL-Std. 883E 3015.7* methods
Latch-Up		100	mA	*@85°C, JEDEC 78*
Thermal Resistance Θ_{JA}		201.7	ºC/W	on PCB
Operating Temperature Range	-40	+85	ºC	
Junction Temperature		+150	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

V_{IN} = V_{OUT} + 0.5V, V_{OUT} = 2.85V, *C_{IN} = C_{OUT} = 1µF, T_{AMB} = -40°C to +85ºC (unless otherwise specified). Typ values are at T_{AMB} = +25ºC.*

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2		5.5	V
ΔV_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, T_{AMB} = +25ºC	-1		+1	%
		I_{OUT} = 100µA to 200mA, T_{AMB} = +25ºC	-1.5		+1.5	
		I_{OUT} = 100µA to 200mA	-2.5		+2.5	
I_{OUT}	Maximum Output Current	each channel	200			mA
I_{GND}	Ground Current	one channel on, I_{OUT} = 50µA		25	50	µA
		one channel on, I_{OUT} = 200mA		30	55	µA
I_{LIMIT}	Current Limit	OUT = short	210	300	400	mA
	Dropout Voltage [1]	2.5V ≤ V_{OUT} < 3V, I_{OUT} = 100mA		60	120	mV
I_Q	Quiescent Current	both channels on, I_{OUT} = 0.05mA		30	90	µA
		both channels on, V_{IN} = V_{OUTNOM} - 0.1V, I_{OUT} = 0mA		50		
V_{LNR}	Line Regulation	V_{IN} = (V_{OUT} +0.5V) to 5.5V, I_{OUT} = 1mA		0.02		%/V
V_{LDR}	Load Regulation	I_{OUT} = 1 to 200mA		0.0005		%/mA
I_{SHDN}	Shutdown Current	OUT 1 and OUT 2 disable		0.01	2	µA
PSRR	Ripple Rejection	f = 1kHz, I_{OUT} = 10mA		85		dB
		f = 10kHz, I_{OUT} = 10mA		65		
		f = 100kHz, I_{OUT} = 10mA		50		
	Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LOAD} = 20mA		20		µV
Enable						
	Enable Input Bias Current			0.01		µA
	Enable Exit Delay [2]	both channels initially off		150		µs
		one channel initially off		200		
	Enable Logic Low Level				0.4	V
	Enable Logic High Level		1.4			V
Thermal Protection						
T_{SHDN}	Thermal Shutdown Temperature			160		ºC
ΔT_{SHDN}	Thermal Shutdown Hysteresis			15		ºC

1. Dropout is defined as V_{IN} - V_{OUT} when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
2. Time needed for V_{OUT} to reach 90% of final value.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

VIN = VOUT + 0.5V, VOUT = 2.85V, CIN = COUT = 1µF, TAMB = 25°C (unless otherwise specified).

Figure 3. Output Voltage vs. Temperature

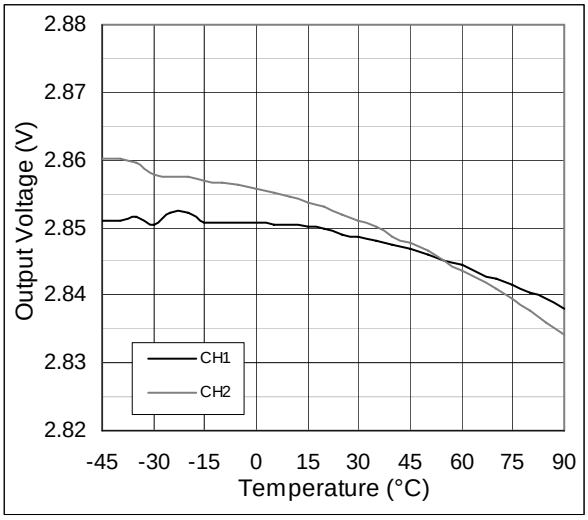


Figure 4. Output Voltage vs. Input Voltage

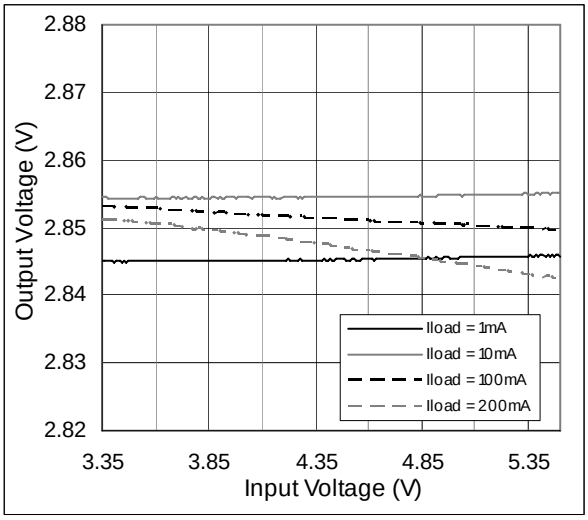


Figure 5. Output Voltage vs. Load Current

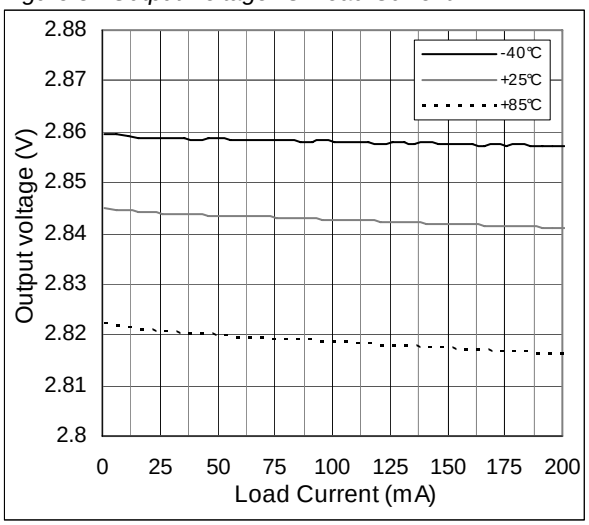


Figure 6. Output Voltage vs. Input Voltage - Dropout

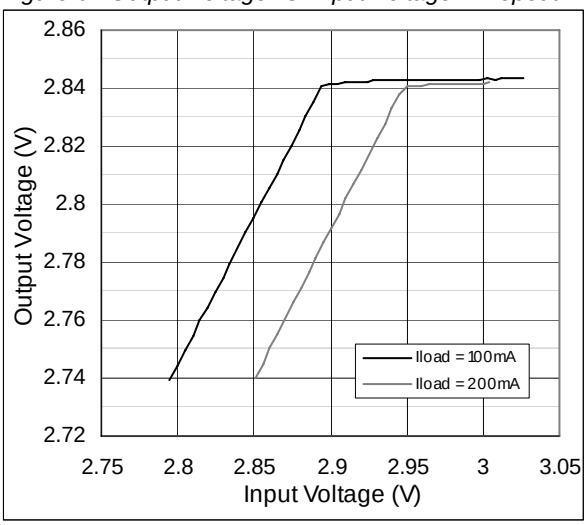


Figure 7. Dropout Voltage vs. Load Current

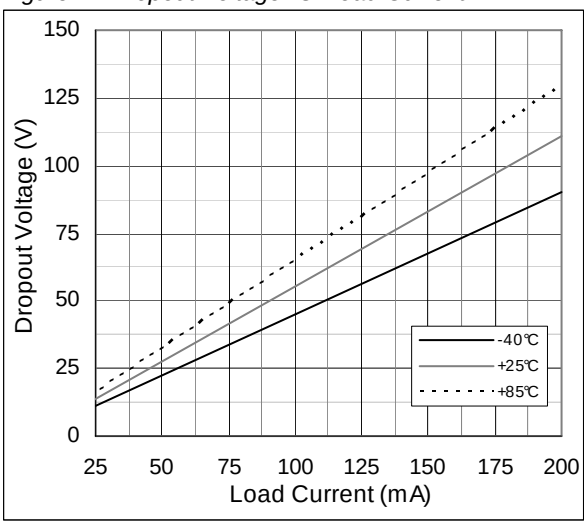


Figure 8. PSRR vs. Frequency

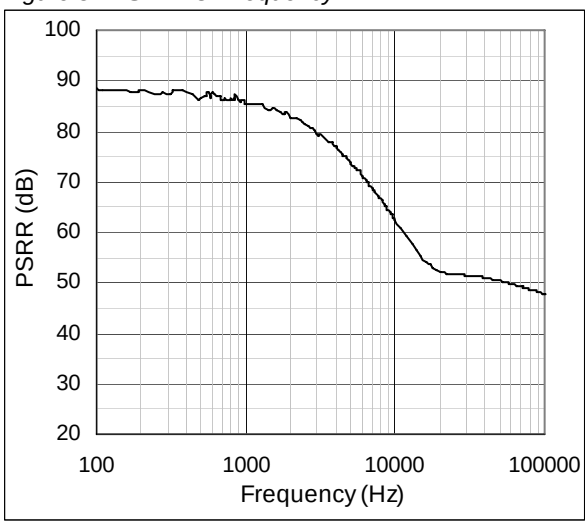


Figure 9. Ground Pin Current vs. Load Current

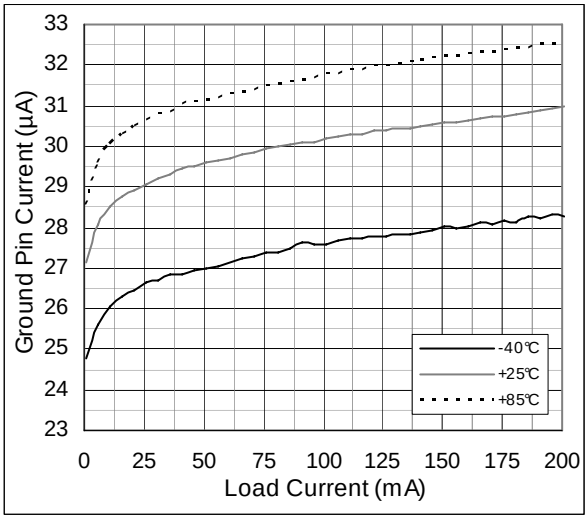


Figure 10. Ground Pin Current vs. Temperature

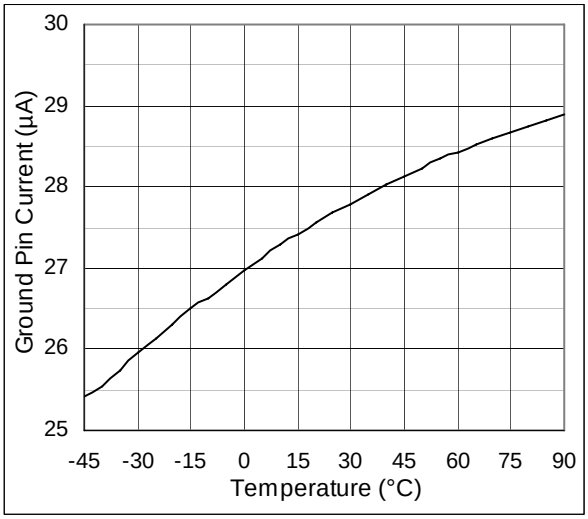


Figure 11. Ground Pin Current vs. Input Voltage; one Channel on, no Load

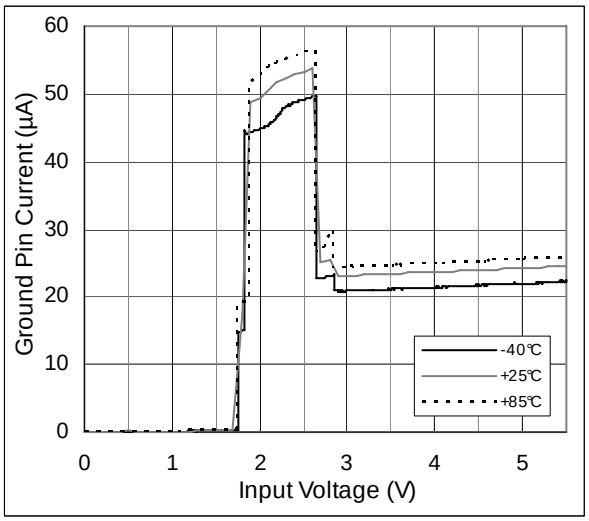


Figure 12. Ground Pin Current vs. Input Voltage; one Channel on, I_{LOAD} = 200mA

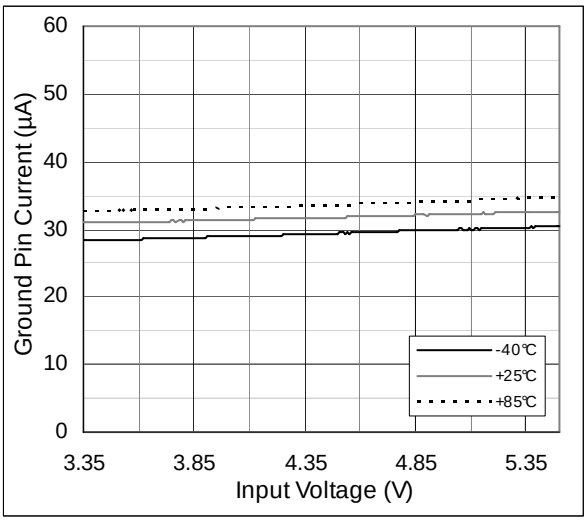


Figure 13. Ground Pin Current vs. Input Voltage; both Channels on, no Load

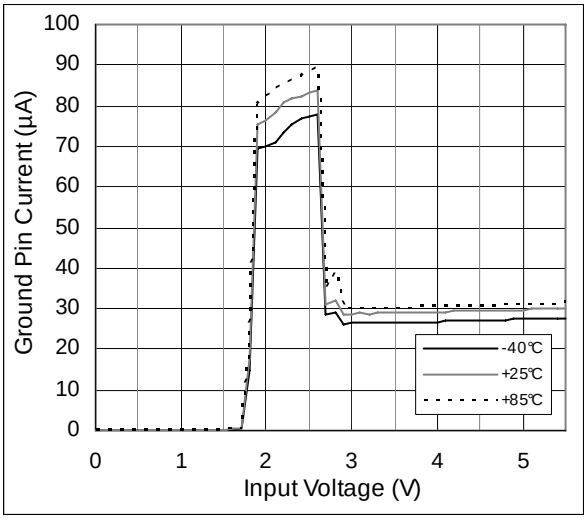


Figure 14. Ground Pin Current vs. Input Voltage; both Channels on, I_{LOAD} = 200mA

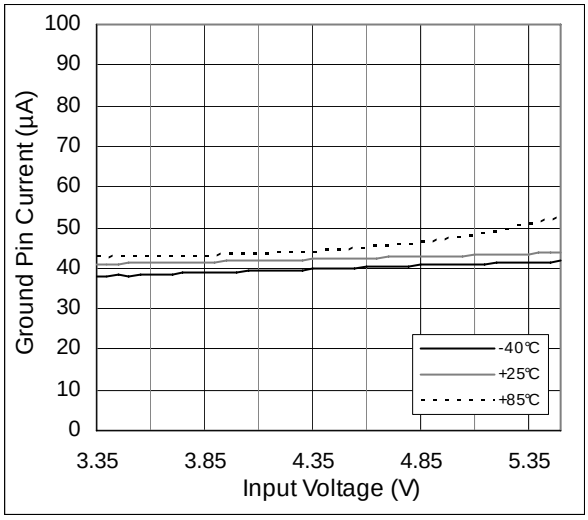


Figure 15. Shutdown Current vs. Input Voltage

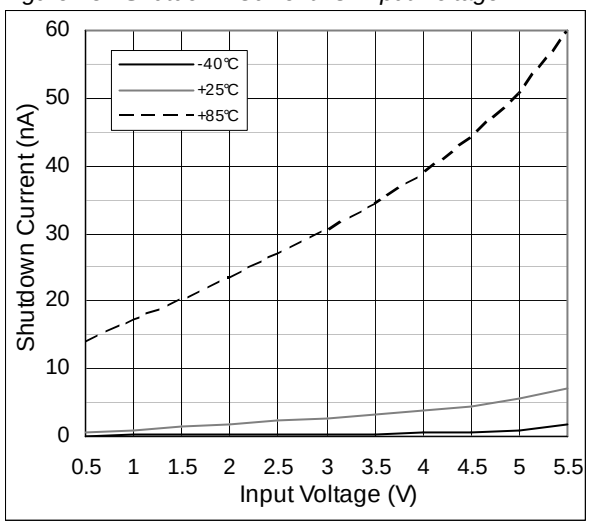


Figure 16. Load Regulation vs. Temperature

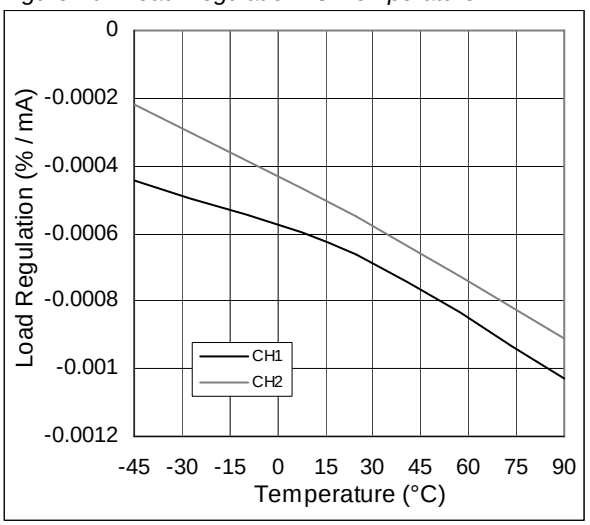


Figure 17. Line Regulation vs. Load Current

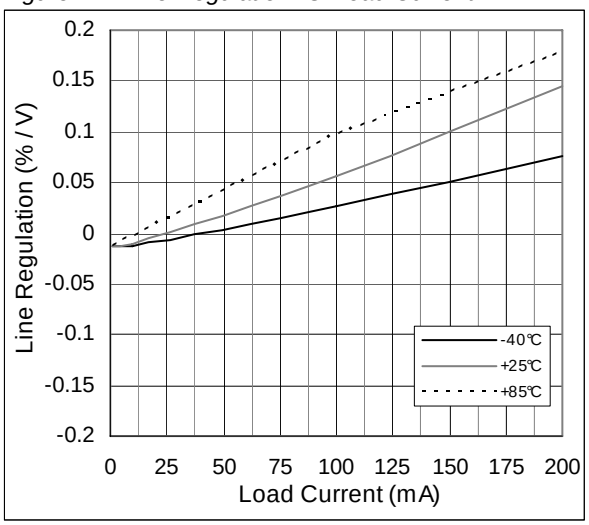


Figure 18. Line Regulation vs. Temperature

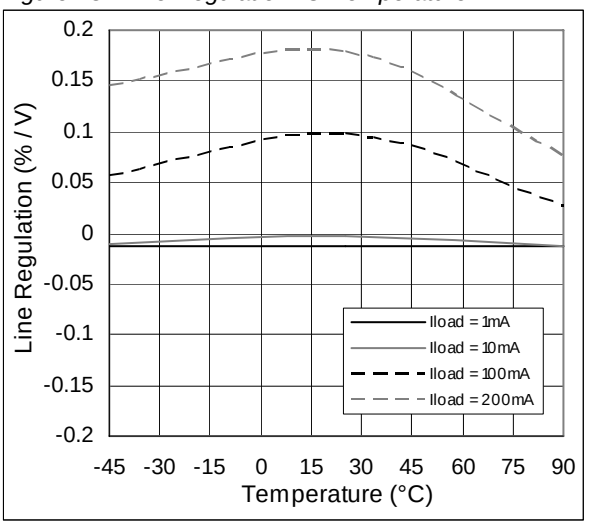


Figure 19. Load Transient Response, Crosstalk, between CH1 and CH2, I_{OUT} = 200mA

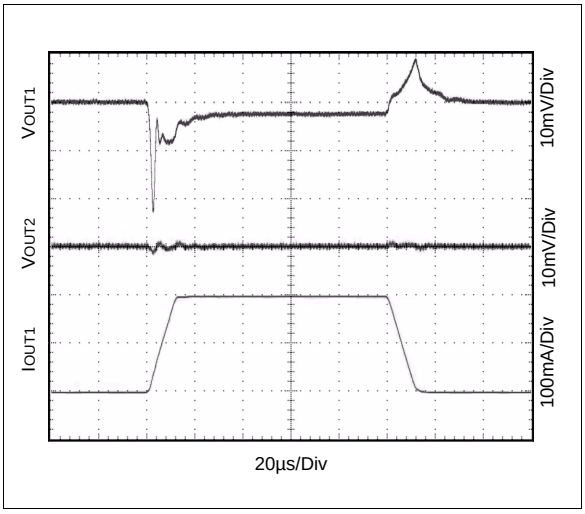


Figure 20. Load Transient Response near Dropout, I_{OUT} = 200mA

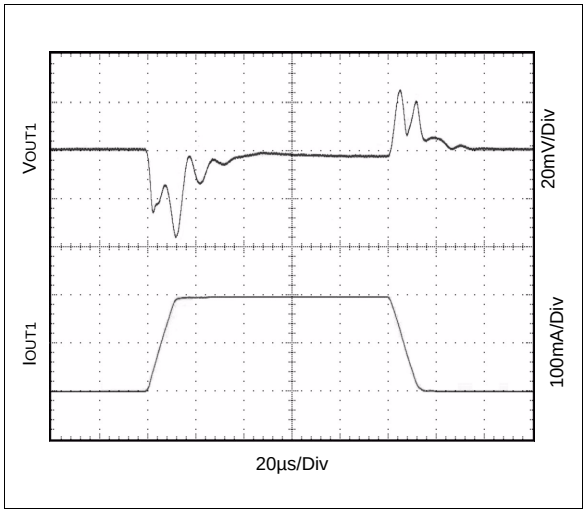


Figure 21. Line Transient Response

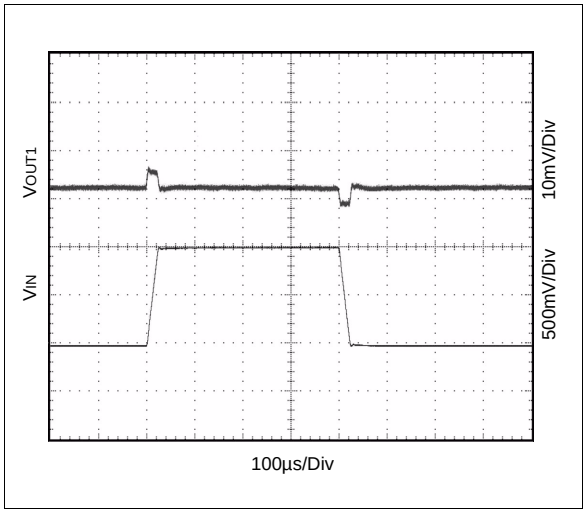


Figure 22. Shutdown

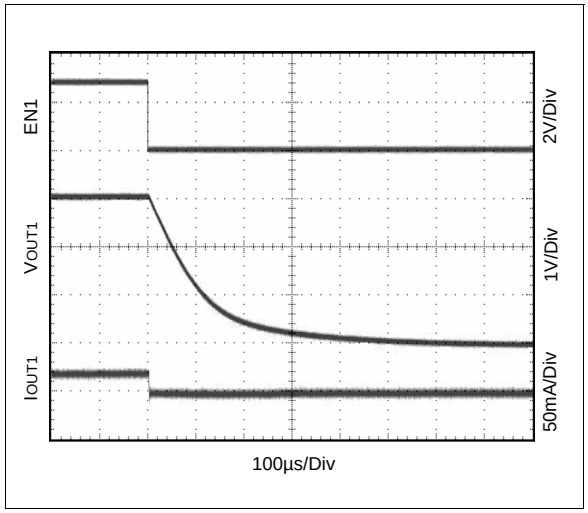


Figure 23. Startup of CH1 when CH2 is Off

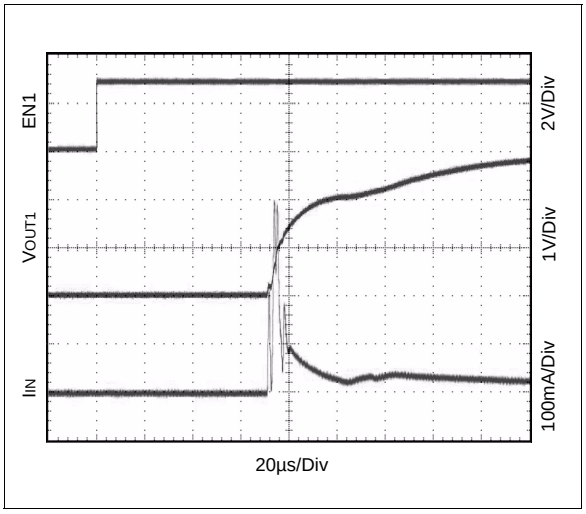
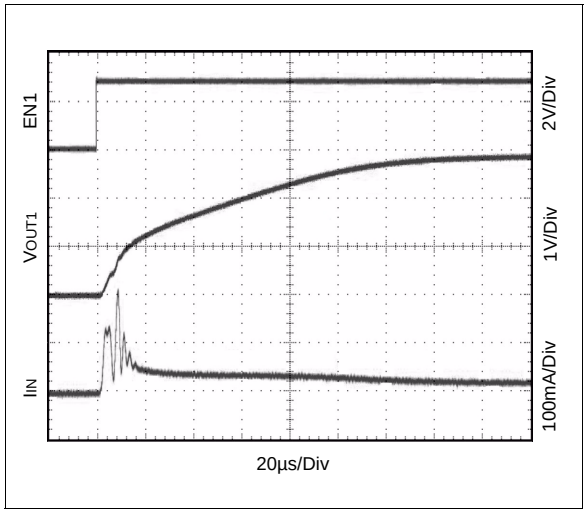


Figure 24. Startup of CH1 when CH2 is On



8 Detailed Description

The AS1374 is an ultra-low-noise, low-dropout, low-quiescent current linear-regulator with two seperated outputs specifically designed for space-limited applications. These device can supply loads up to 200mA. As shown in Figure 25, the AS1374 consist of an integrated bandgap core, error amplifier, P-channel MOSFET pass transistor, and internal feedback voltage-divider.

The output voltage is fed back through an internal resistor voltage-divider connected to pin OUT. Additional blocks include a current limiter, thermal sensor, and enable logic.

Internal Voltage Reference

The bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output.

Internal P-Channel Pass Transistor

The AS1374 feature a 0.6Ω (typ) P-channel MOSFET pass transistor, which provides several advantages over similar designs using a PNP pass transistor, including prolonged battery life. The P-channel MOSFET does not require a base driver, thus quiescent current is dramatically reduced. The AS1374 do not exhibit problems associated with typical PNP-based LDOs, and consume only 30µA of quiescent current in light load and 50µA in dropout (see Typical Operating Characteristics on page 5).

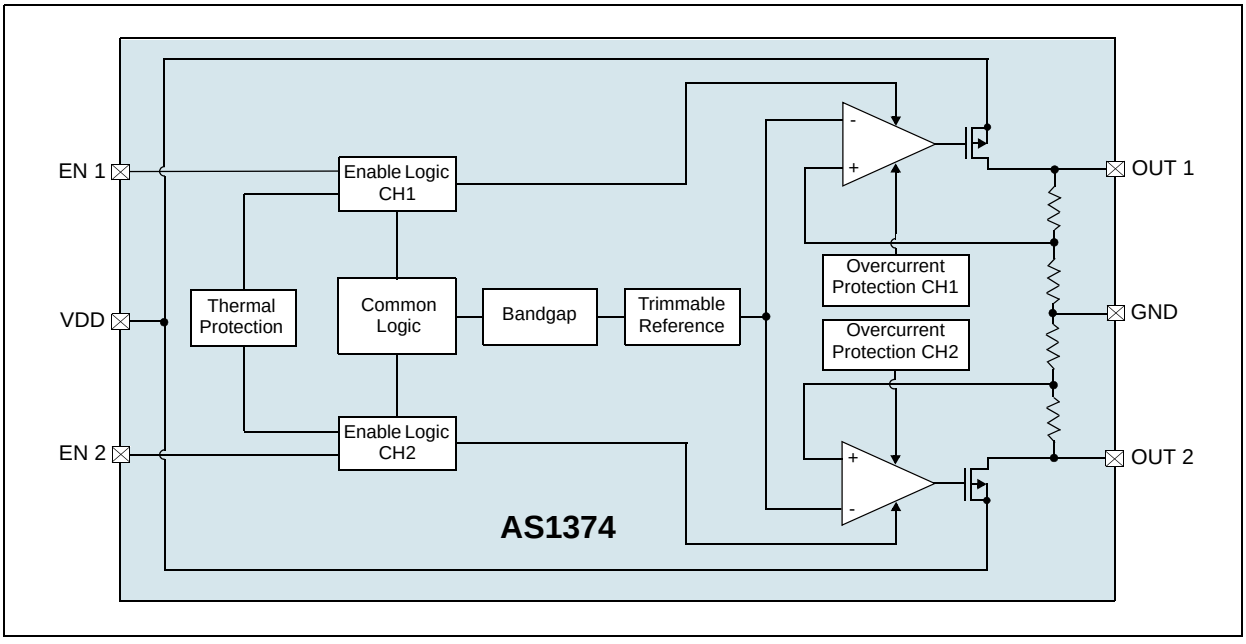
Output Voltage

The AS1374 deliver preset output voltages from 1.2V to 3.6V, in 50mV increments (see Ordering Information on page 13).

Enable

The AS1374 feature an actice high enable mode to shutdown each output indepentend. Driving EN 1 low disables Output 1, driving EN 2 low disables Output 2. The disabled Output enters a high-impedance state.

Figure 25. AS1374 - Block Diagram



Current Limit

The AS1374 include a current limiting circuitry to monitor and control the P-channel MOSFET pass transistor's gate voltage, thus limiting the device output current to 300mA.

Note: See Table 3 on page 4 for the recommended min and max current limits. The output can be shorted to ground indefinitely without causing damage to the device.

Thermal Protection

Integrated thermal protection circuitry limits total power dissipation in the AS1374. When the junction temperature (T_J) exceeds +160ºC, the thermal sensor signals the shutdown logic, turning off the P-channel MOSFET pass transistor and allowing the device to cool down. The thermal sensor turns the pass transistor on again after the device's junction temperature drops by 15ºC, resulting in a pulsed output during continuous thermal-overload conditions.

Note: Thermal protection is designed to protect the devices in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150ºC.

Operating Region and Power Dissipation

The AS1374 maximum power dissipation is dependant on the thermal resistance of the case and PCB, the temperature difference between the die junction and T_{AMB}, and airflow rate.
Power dissipation across the device is calculated as:

$$PD = I_{OUT} (V_{IN} - V_{OUT}) \quad (EQ\ 1)$$

The maximum power dissipation is calculated:

$$PDMAX = (T_J - T_{AMB})/\theta_{JA} \quad (EQ\ 2)$$

Where:
$T_J - T_{AMB}$ is the temperature difference between the AS1374 die junction and the surrounding air;
θ_{JA} is the thermal resistance through the circuit board, copper traces, and other materials to the surrounding.

9 Application Information

Capacitor Selection and Regulator Stability

For normal operation, use a 1µF capacitor at pin VDD and a 1µF capacitor at pin OUT. Larger input capacitor values and lower ESR provide better noise rejection and line-transient response. Reduce output noise and improve load-transient response, stability, and power-supply rejection by using large output capacitors.

Note: Some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use a 2.2µF or larger output capacitor to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1µF is sufficient at all operating temperatures.

Noise, PSRR, and Transient Response

The AS1374 is designed to deliver ultra-low noise and high PSRR, as well as low dropout and low quiescent currents in battery-powered systems. The power-supply rejection is 85dB at 1kHz and 50dB at 100kHz. (see Figure 8 on page 5).

When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors, and through passive filtering techniques.

The Figure 19, Figure 20 on page 7 and Figure 21 on page 8 show the AS1374 Load- and Line- Transient Responses.

Dropout Voltage

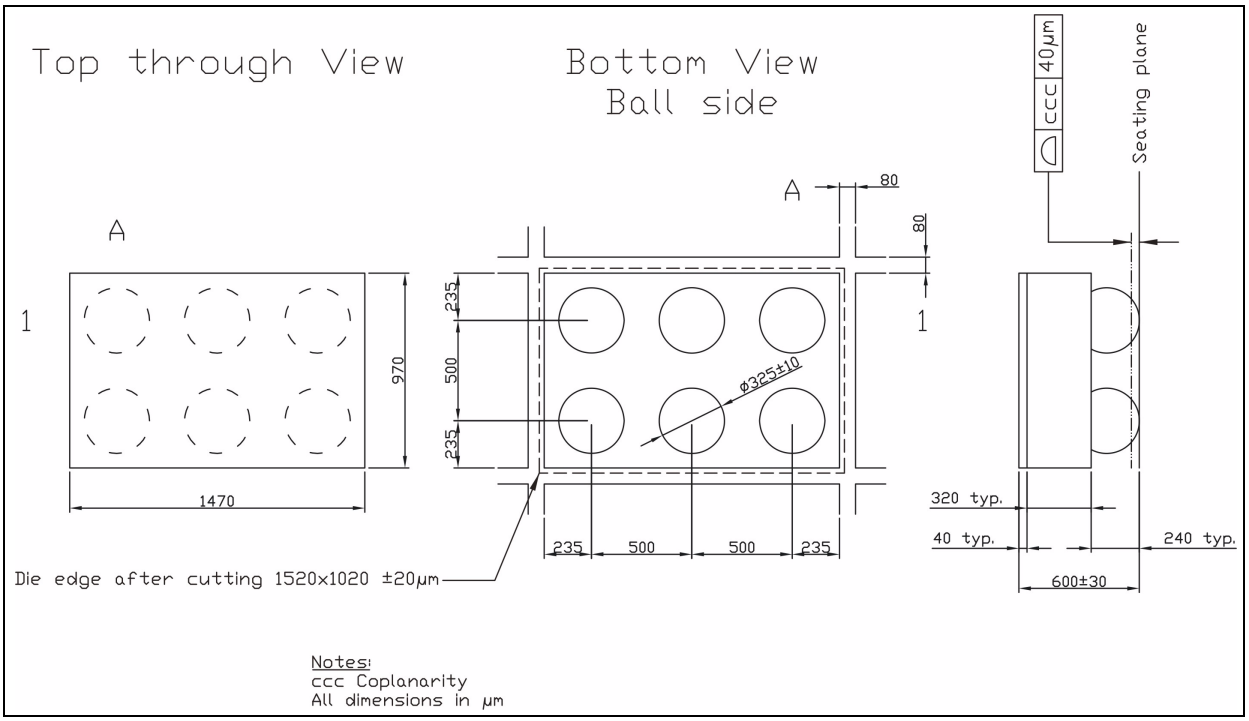
The AS1374 minimum dropout voltage determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage.

Since the AS1374 use a P-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by I_{LOAD} (see Figure 7 on page 5).

10 Package Drawings and Markings

The devices are available in a 6-bump WLP package.

Figure 26. 6-bump WLP Package



11 Ordering Information

The devices are available as the standard products shown in Table 4.

Table 4. Ordering Information

Ordering Code	Marking	Output Voltage 1	Output Voltage 2	Delivery Form	Package
AS1374-BWLT-285	ASSH	2.85V	2.85V	Tape and Reel	6-bump WLP
AS1374-BWLT1833	ASSJ	1.8V	3.3V	Tape and Reel	6-bump WLP
AS1374-BWLT1218	ASSK	1.2V	1.8V	Tape and Reel	6-bump WLP

Non-standard devices from 1.2V to 3.6V are available in 50mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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